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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/537,516	06/03/2005	Alan G Knapp	GB02 0215 US	4656

24738 7590 03/05/2008

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EXAMINER	
RAINEY, ROBERT R	
ART UNIT	**PAPER NUMBER**
2629	

MAIL DATE	DELIVERY MODE
03/05/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/537,516	KNAPP ET AL.	
	Examiner	Art Unit	
	ROBERT R. RAINEY	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 6-30-05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because the unlabeled rectangular boxes shown in the drawings should be provided with descriptive text labels. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.
    (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Examiner encourages the applicant to add the headings for items (f) to (j).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,618,111 to *Nagata et al.* ("*Nagata*") in view of U.S. Patent No. 6,646,425 to *Miftakhutdinov* ("*Miftakhutdinov*").

As to **claims 1 and 5**, *Nagata* discloses an LCD display device with means to mitigate the effects of voltage drop caused by wire resistance (see for example column 3 line 65 to column 4 line 8) and in particular:

An integrated circuit arrangement comprising:

a plurality of integrated circuit modules (see for example Fig. 1 items 5 and column 6 lines 7-16 and for example items 7, 4a, and any other modules as described since nothing in the claim precludes some of the plurality of modules from being different from the one described below);

a first power line (see for example column 5 lines 21-25 "GND");

a second power line (see for example column 6 lines 52-58 "Vcc");

an integrated circuit module (see for example Fig. 1 items 5 and column 6 lines 7-16) from the plurality of circuit modules comprising:

an internal power line (see for example column 6 lines 54-58 "3.3 V");

and a circuit module portion coupled between the first power line and the internal power line (see for example Fig. 1 items 5 and column 6 lines 54-58 "source TCP 5");

the integrated circuit arrangement further comprising a voltage generator (see for example column 6 lines 54-58 "regulator" described as being part of Fig. 1 items 7) coupled between the first power line and the second power line (see

for example column 6 lines 54-58, which explicitly states that the regulator is mounted, i.e. coupled, to the Vcc wire, i.e. the second power line; the connection to GND, i.e. the first power line (is not stated but would be fairly suggested to one skilled in the art at the time of the invention), the voltage generator having an output (see for example column 6 lines 54-58 "3.3 V") coupled to the internal power line.

Nagata does not expressly disclose a reference power line and the voltage generator having a control terminal coupled to the reference power line.

Miftakhutdinov discloses a distributed power arrangement for electronic panels and in particular: a reference power line and a voltage generator having a control terminal coupled to the reference power line (see for example Fig. 4 item 126 "external reference voltage" column 7 line 3, which is shown to be connected to items 118 "voltage regulator system" column 7 line 2). Note also that *Miftakhutdinov* discloses all claimed limitations except that a power "plane" is described associated with the first power as opposed to a "line" (see for example Fig. 4 and column 6 line 47 to column 7 line 12).

Nagata and *Miftakhutdinov* are analogous art because they are from the same field of endeavor, which is distributed power supplies for electronic panels, and seek to solve the same problem, which is to overcome the adverse effects of voltage droop caused by the impedance of power conductors.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to enhance the system after *Nagata* with the reference

power line disclosed by *Miftakhutdinov*. The suggestion/motivation would have been to provide advantages such as to ensure that all output voltages would be substantially equal (see for example column 6 lines 64-67).

As to **claim 2**, in addition to the rejection of claim 1 over *Nagata* and *Miftakhutdinov*:

Nagata and *Miftakhutdinov* disclose the claimed invention except for the integrated circuit module from the plurality of integrated circuit modules further comprising a second circuit module portion coupled between the first power line and the second power line. *Miftakhutdinov* discloses that it is known in the art to provide different supply voltages to different circuit module portions with characteristics as required by the powered circuitry (see for example column 1 lines 34-40). It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the device of *Nagata* and *Miftakhutdinov* with circuit module portions connected to power supplies matching the requirements of the circuit module portions as suggested by *Miftakhutdinov* including connecting circuit module portions as claimed, in order to provide the circuit module portions with the appropriate power or to save cost or power by avoiding unnecessarily exact regulation.

As to **claim 3**, in addition to the rejection of claim 1 over *Nagata* and *Miftakhutdinov*, *Miftakhutdinov* further discloses that the voltage regulator

provides an output voltage substantially equal to the reference voltage (see for example column 6lines 66-67).

Nagata and *Miftakhutdinov* disclose the claimed invention except for the voltage generator comprising an operational amplifier having a non-inverting input comprising the control terminal and an inverting input coupled to the internal power line. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use an amplifier so connected as the since it was known in the art to use an op-amp connected as described to buffer a reference voltage (as evidence that this was known, see for example U.S. Patent No. 6,762,565 to Kudo et al. Fig. 2 items 106 and 107).

As to **claim 4**, in addition to the rejection of claim 1 over *Nagata* and *Miftakhutdinov*, *Nagata* further teaches an active matrix substrate, which includes a TFT (see for example Fig. 1 item 8); and *Miftakhutdinov* further discloses a current sharing (see for example column 4 lines 46-50, obvious to have a current source).

Nagata and *Miftakhutdinov* disclose the claimed invention except for the voltage generator comprising: a current source coupled between the first power line and the internal power line; and a transistor coupled between the internal power line and the second power line, the transistor having a gate comprising the control terminal. It would have been an obvious matter of design choice for the

current source and the transistor to be coupled between the power source and the internal power lines.

As to **claim 9**, in addition to the rejection of claim 1 over *Nagata* and *Miftakhutdinov*, *Miftakhutdinov* further discloses an electronic device comprising the integrated circuit arrangement of claim 1 and having power supply means coupled to the first power line, the second power line (see for example column 6 lines 30-32) and the reference power line (see for example Fig. 4 item 126 "external reference voltage" column 7 line 3) of the integrated circuit arrangement.

As to **claims 6 and 10**, the same rejection as for claim 9 above except, *Nagata* further discloses the electronic device further comprising a matrix array device, the matrix array device comprising: a first set of conductors (see for example Fig. 1 conductors connected to items 5a); a second set of conductors (see for example Fig. 1 conductors connected to items 4a), the conductors from the second set of conductors being substantially perpendicularly oriented to the conductors from the first set of conductors, a plurality of matrix elements, each matrix element from the plurality of matrix elements being coupled between a conductor from the first set of conductors and a conductor from the second set of conductors (see for example column 5 lines 30-43), at least one of the conductors from the first set of conductors or the second set of conductors being

coupled to an integrated circuit module from the plurality of integrated circuit modules (see for example column 6 lines 13-17).

As to **claim 7**:

Claim 6 claims an integrated circuit arrangement with a circuit portion having an output coupled to a conductor from a **first** set of conductors. Claim 7 adds a second integrated circuit arrangement with identical limitations except that it includes a circuit portion having an output coupled to a conductor from a **second** set of conductors.

In addition to the rejection of claim 6 over *Nagata* and *Miftakhutdinov*: *Nagata* further discloses multiple instances of the integrated circuit arrangement (see for example Fig. 1, ibid.) and circuit portions coupled to conductors from a second set of conductors (see for example Fig. 1 items 4a).

Nagata and *Miftakhutdinov* disclose the claimed invention except for the voltage buffering being provided to the drivers for the second set of conductors. The claimed improvement would have been obvious to one of ordinary skill in the art at the time of the invention since one of ordinary skill could have applied the known improvement technique in the same way to the drivers for the second set of conductors and the results would have been predictable to one of ordinary skill in the art.

As to **claim 8**, in addition to the rejection of claim 6 over *Nagata* and *Miftakhutdinov*, *Nagata* further discloses that the matrix array device is a display device (see for example column 1 lines 5-10).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. 6,690,149 to Monomoushi et al. discloses various voltage buffer arrangements for displays.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT R. RAINEY whose telephone number is (571)270-3313. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RR/

AMARE MENGISTU
SUPERVISORY PATENT EXAMINER